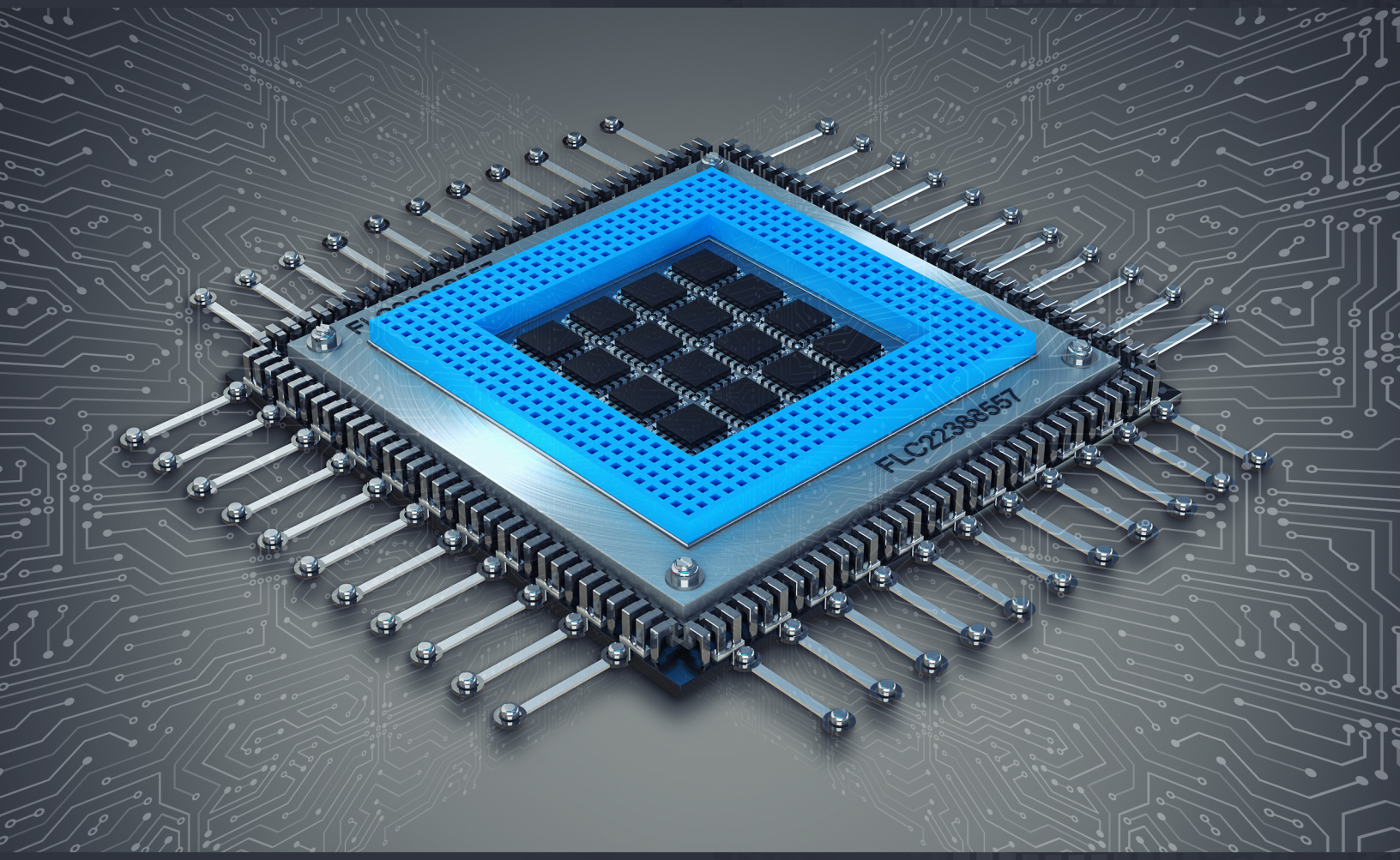
SOLID STATE & MICROELECTRONICS TECHNOLOGY



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Solid State & Microelectronics Technology

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ISBN (Online): 978-981-5079-87-6

ISBN (Print): 978-981-5079-88-3

ISBN (Paperback): 978-981-5079-89-0

First published in 2023.

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CONTENTS

PREFACE

Solid-state and Microelectronics technology attempts to fill the gap between a general solid-state physics book and real-life application by providing detailed explanations of the electronic, vibrational, transport and optical properties of semiconductors. The approach is physical and instinctive rather than prescribed. The enhanced application of semiconductors to the different electronic industries helped to explore various aspects of microelectronics technology which was made possible with the availability of solid-state devices known for their versatile applications.

This technological advancement also demanded the proper understanding of new device physics as the properties of materials alters significantly at this reduced dimension. These dimensions are comparable to the electron wavelength of motion, and hence the device characteristics are governed by the confinement of the electron wave function, commonly referred to as the quantum confinement effect.

For the purpose of commercialization, integration of different electronic components on the same platform is very much essential to develop an integrated device using a standard IC fabrication process. Thus, low power, low cost, highly sensitive and miniaturized electronic system on chip using silicon is possible. This book consists of thirteen chapters.

The most apparent package for PART I consists of chapter 1 to 6, and PART II consists of chapter 7 to 12. The goal was to give a brief idea about the microfabrication technology needed to fabricate solid-state devices through part II.

Chapter 1 provides an introduction to Semiconductor Physics fundamentals. Basic quantum mechanics have been introduced in order to explain the fundamental properties of semiconducting materials. In this context, Sommerfeld's free electron theory has been considered. Although this model corroborates with a few experimental observations, but can't differentiate between semiconductors, insulators and metal. Then Kronig – Penney, who successfully explains the deviation on the basis of the band concept, has been considered. Followed by Kronig – Penney model, Bloch's theory has been introduced, and it well explains the origin of conduction and valence bands. From this concept, different types of semiconducting materials, *e.g*., direct and indirect band gap semiconductors, n- and p-type semiconductors, *etc*., have emerged. Here,

properties of charge carriers, such as their charge, effective mass, *etc*., have also been discussed. Knowing these parameters, conductivity expression and related scattering phenomena influencing conductivity have been briefly elaborated.

Chapter 2 briefly discusses the fundamentals of the p – n junction, the electric field across the junction, equilibrium carrier concentration on each side, *etc*. Expression of built-in potential in terms of carrier density has been derived. Magnitudes of the current under zero, forward, and reverse biased conditions have been calculated. Unlike a resistor, p – n junction corresponds to static, dynamic and average ac resistance, and they have been briefly discussed here along with protocol to examine their values. These p – n junctions also exhibit capacitance, namely transition capacitance and diffusion capacitance. Herein, these parameters and their relevance in terms of current-voltage characteristics of p – n junction and applicational aspects, have been elaborated.

Chapter 3 discusses metal-semiconductor contacts. Schottky and Ohmic contact with a detailed band diagram has been presented. I-V characteristics are also given to interpret the contact behaviour.

Chapter 4 deals with JFET and its I-V characteristics expressed in a detailed manner with necessary equations. JFET parameters are another important factor to understand the characteristics of it which have been mentioned. Small signal model of JFET illustrated in a very lucid manner.

Chapter 5 discusses the fabrication of MOSFET and its principle operations based on the concept of metal-oxide-semiconductor technology. Further the discussion is focused on the details mathematical modelling of MOS capacitors, device characteristics and the process of channel length modulation and its application. The conversation is continuing on the concept of CMOS technology and its combination with the transistor – the BiCMOS technology.

Chapter 6 discusses advanced semiconductor devices where Semiconductor resistivity can be changed by the incorporation of an electric or magnetic field, by revelation to light or heat, or by mechanical distortion. The doping of silicon significantly modulates the characteristics of semiconductors to have different types of devices like LED, Tunnel diode, Solar cells and many more, which have been discussed in this section.

Chapter 7 introduces silicon as an electronic material for microelectronic device fabrication. It discusses, in-depth, the various aspects of crystalline silicon, wafer

manufacturing and their identification techniques. Finally, the various steps involved in a microfabrication process are also discussed. From this chapter, the readers are expected to learn how to process a silicon wafer successfully and proceed with customized device fabrication.

Chapter 8 introduces the readers to the oxidation process focusing on silicon. It establishes the importance of oxidation in a silicon process and discusses in depth the thermal oxidation process and its growth mechanism. Towards the end, a detailed discussion of the oxide film characterization and its properties has been provided. After reading this chapter, the readers are expected to have a sound knowledge of the oxidation process as a whole and its significance in the silicon processing industry.

Chapter 9 introduces the readers to the diffusion process which is used for doping intrinsic silicon. It discusses in depth Fick's Law of diffusion and the different types of diffusion that may be observed. Towards the later part of the chapter, the process of diffusion in semiconductors is discussed in detail, explaining the diffusion-assisted doping process commonly employed for semiconductors, especially silicon.

Chapter 10 discusses in depth the ion implantation process of silicon processing technology. The chapter gives an in-depth insight into various aspects of the ion implantation process and ion-implanted silicon systems commonly encountered in a silicon process. The readers, after reading this chapter, will have a sound understanding of the ion implantation process and its various aspects.

Chapter 11 represents the concept of MEMS technology. Fabrication technique, including bulk and surface micromachining with CMOS compatibility issues, has been elaborated. The most important etch-stop techniques have also been elaborated in this chapter.

Chapter 12 provides the idea about photo-resist, and its properties. It also narrates some advanced lithographic techniques, including the most common one, optical lithography.

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CHAPTER 1

Fundamentals of Semiconductor Physics

Abstract: In recent times, crystalline semiconductors have played a major role in device fabrication for all purposes, where crystal structure plays the most crucial role. Herein, all kinds of fundamental unit cell structures have been briefly discussed, whereas Miller indices have been introduced to illustrate the orientation of the crystal structures. Basic quantum mechanics have been introduced in order to explain the fundamental properties of semiconducting materials. In this context, Sommerfeld' free electron theory has been considered. Although this model corroborates with a few experimental observations, but can't differentiate between semiconductors, insulators and metals. Then Kronig – Penney, which successfully explains the deviation on the basis of the band concept, has been considered. Following the Kronig – Penney model, Bloch's theory has been introduced, and it well explains the origin of conduction and valence bands. From this concept, different types of semiconducting materials, e.g., direct and indirect band gap semiconductors, n- and p-type semiconductors, *etc*., have emerged. Here, properties of charge carriers, such as their charge, effective mass *etc*., have also been discussed. Knowing these parameters, conductivity expression and related scattering phenomena influencing conductivity have been briefly elaborated.

Keywords: Band, Crystal structure, Fermi – Dirac statistics, Scattering, Semiconductor.

INTRODUCTION

A semiconductor is a sub-group of materials with electrical conductivity between metal and insulators. The parameter which differentiates semiconductors from metal and insulator others is the band gap of reasonable value. Unlike metal and insulators, the electrical conductivity of semiconducting materials is very sensitive to temperature and easily tunable, and thus they have been attracted due to their opportunities in various devices. Though the study of semiconductors started in the year 1930, the real essence of semiconducting materials came when the transistor was invented in the year 1947. Later, with the invention of silicon bipolar transistors, semiconductor devices grow rapidly. After successful integration with computers in the late 1970 – 1980s, the demand for semiconductor materials with memory effect had increased dramatically. Late in the 1960s and 1970s, Leo Esaki and his peer group developed a new crystal growth method, molecular beam epitaxy, to develop semiconducting materials, which opened new concepts of quantum well, superlattice based semiconducting devices [1]. In the late 1980s, the concept of high-mobility transistors came up and triggered a wide variety of applications, including superlattice-based receivers for satellite broadcasting.

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Besides Si-based large-scale integrated memory, metal-semiconductor field-effect transistors (MESFET) based GaAs had emerged as an important material for mobile phones in the 1990s. Till then, GaAs became a boom for next-generation technology in the 21st century. After the discovery of the quantum Hall effect, also known as the integer quantum Hall effect, two-dimensional electron gas systems of semiconducting materials opened new applicational opportunities. During the last decade, the fractional quantum Hall effect came into the picture with its several scopes. Recently, we have technologies to fabricate various micro- and nanostructures of semiconducting materials that give several new quantum phenomena like Aharonov-Bohm, ballistic transport, electronic interference, *etc.* In recent times, many technologies have emerged out of these phenomena. It is very well known to all of us that semiconductors play an important role in information technology and all kinds of electronic gadgets around us, such that we can't talk about anything without semiconductor devices. Herein, it may be stated that the performances of semiconductor-based devices and related technologies significantly depend on several physical parameters of the semiconducting materials. Therefore, to explore different technological aspects and devices of these semiconducting materials, we have to understand their basic physics. Early initiatives were taken around the 1950s to understand the optical and electrical properties of semiconducting materials, and it was resolved during the 1960s that all the fundamental properties of the semiconducting materials were related to energy band structures which is nothing but energy (E) – wave vector (k) relation, called E(k) diagram, for the electrons within semiconducting materials. In fact, this band structure allows us to differentiate between an insulator, a semiconductor and a metal. In this context, it may be stated that the microscopic properties of electrons are conveniently described by band structure. During 1955s, cyclotron resonance experiments carried out on semiconducting materials, gave the first experimental information about the E(k) diagram of the valence band, *i.e*., the lowest occupied energy levels of semiconducting materials. This experiment also revealed the existence of degeneracy of valence bands and successively concepts of two types of holes, *i.e*., heavy-hole and light-hole bands. In this context, it may also be noted that there were several controversies during the early stage of the development of semiconductor-based devices. For example, when transistors were invented, it was unclear whether germanium was direct or indirect band gap semiconducting material. Later on, researchers adopted versatile tools for detailed, in-depth information about the band structure of semiconducting materials. In the present time, several optical and electronic spectroscopic techniques like UV-Vis spectroscopy, photoluminescence spectroscopy, cathodoluminescence spectro scopy, x-ray photoelectron spectroscopy *etc.*, are used to obtain information about band structure experimentally. Herein, it may be stated that in addition to

experimental processes, several empirical pseudopotential and quantum mechanical perturbation methods had been simultaneously developed for a theoretical understanding of the band structure of the semiconducting materials. Among them, k·p and Kronig – Penny technique, developed during late 196os, became the most popular. Presently, density functional theory is being widely used to calculate band structure and related optical, electrical and magnetic properties of semiconducting materials. Herein, it may be stated that the band structure of any semiconducting material is crucial as it determines every property, hence every applicational possibility of the semiconducting materials depends on the band structure. Therefore, we have to understand the fundamental of the band structure of semiconducting materials, which is mainly carried out by solving Schrödinger's equation. However, solving Schrödinger's equation to understand electron behavior in a semiconducting material with ~ 10^{23} atoms/cm^3 is very complicated. To simplify this tedious job, symmetries of semiconductors that involve translational, rotational and reflection are being utilized. Here, Group theory is the tool that facilitates the task. As our primary objective of this chapter is to understand band structure and related electronic properties, we must have initial knowledge based on the symmetry of the semiconducting materials and group theory. So primarily, these will be discussed, and then band structure, and electronic behavior will be developed.

Classification, Crystal Structure and Miller Indices of Semiconducting Materials

Like, other materials, semiconductors consist of a large number of the same or different types of atoms. However, depending on atomic arrangements, they are broadly classified into three categories: amorphous, single crystalline and polycrystalline. In amorphous semiconductors, there is no long-range ordering of atoms within the materials, and one part has a completely different look from the other part (Fig. **1a**). Atoms are arranged with lone ordering in a single crystalline material in all three directions (Fig. **1b**). Unlike amorphous, all sections of a single crystalline material are identical. Polycrystalline materials lie in between amorphous and single crystalline materials. Briefly, it comprises crystalline subsections that are disjoined relative to one another (Fig. **1c**). Herein, it may be stated all three kinds of the same materials have their own advantages suitable for particular applications [1]. For example, amorphous Si has high-concentration dangling bonds; those in the presence of an electric field produce electron-hole pairs, hence they are very useful for varies switching devices like liquid crystal displays (LCD). In addition, amorphous Si exhibits excellent uniformity during the thin film, which also makes them beneficial to enhance the brightness of LCD

CHAPTER 2

Fundamentals of p – n Junction

Abstract: In this chapter, fundamentals of the p – n junction, electric field across the junction, equilibrium carrier concentration on each side, *etc*., have been briefly discussed. Expression of built-in potential in terms of carrier density has been derived. Magnitudes of the current under zero, forward, and reverse biased conditions have been calculated. Unlike a resistor, p – n junction corresponds to static, dynamic and average ac resistance, and they have been briefly discussed here along with protocol to examine their values. These p – n junctions also exhibit capacitance, namely transition capacitance and diffusion capacitance. Herein, these parameters and their relevance in current-voltage characteristics of p – n junction and applicational aspects have been elaborated.

Keywords: p – n junction, Biasing, capacitance, Built-in-potential, Graded region.

INTRODUCTION

Although semiconductor devices having one type of charge carrier, like photodetector, *etc*., show potentiality in different applications, however, most semiconductor devices use both types of charge carriers; thus, they are constructed of an n- and p-type regions, joined together, and the interfacial boundary is known as p – n junction. Therefore, the p – n junction is the heart of all the p – n diode devices; hence, for a proper understanding of the p – n devices, it is highly essential to have detailed knowledge of the p – n junction.

Physics of p – n Diode: Depletion Region, Built – in –Potential

In the previous chapter, we discussed the p- and n-type semiconducting materials. Diode gets formed when these two types of materials are joined together. The interface between n-and p-type materials is called the p–n junction (Shown in Fig. (**1**)). In this context, it may be stated that this p – n junction leads to various inventions, including diodes, transistors, integrated circuits, *etc*. Thus, a good understanding of the p – n junction is essential for all semiconductor devices.

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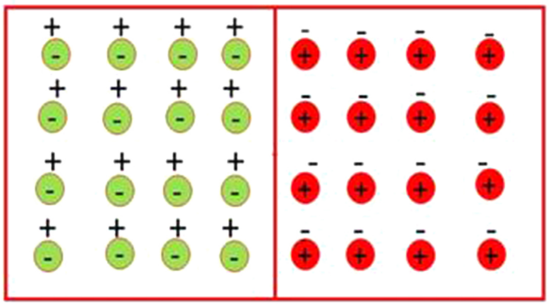

Fig. (1). Schematic view of p – n junction.

As stated in the previous chapter, trivalent atoms are generally used to dope in Si for p-type conductivity, whereas pentavalent atoms are for n-type conductivity. Conventionally, as illustrated in Fig. (**1**), donor ions in the n-type region are represented by a plus sign as they exhibit a positive charge after donating electrons. In contrast, electrons orbiting the donor are characterized by a negative sign. Similarly, acceptors within the p-type region are characterized by a minus sign as they become negatively charged after accepting electrons, and orbiting holes surrounding the acceptor ions are characterized by a positive sign. As both n- and p-type regions are electrically neutral; hence they should be equal in number within each region. In reality, a minor concentration of electrons is present in the p-type region, while a minor concentration of holes exists in the n-type region. Thus, in general, it is stated that electrons are the majority carrier and holes are the minority carrier within the n-type semiconductor. At the same time, reverse distribution happens for the p-type region. Due to the concentration gradient, electrons get diffused into the p-type region from the n-type region, while holes diffuse opposite to reach equilibrium. Electrons immediately recombine because there are so many holes in the p-type region. As a result, immobile acceptor ions within the p-type region carrying negative charge become uncovered. Similarly, hole migration into the n-type region uncovers the positive charge of immobile donor ions (as shown in Fig. (**2**)). These unneutralized Ions in the neighborhood of the p – n junction is uncovered charges [1].

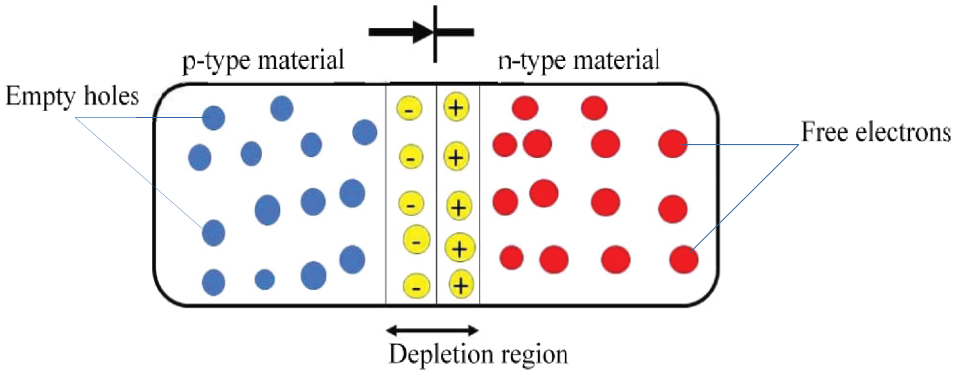

Fig. (2). Schematic diagram of a p – n junction. The yellow portion denotes the depletion region.

Since this region is depleted of free charges, it is often referred to as the depletion region, the space-charge region, or the transition region. It has been noted that the depletion region corresponds very narrow width on both sides of the junction, and beyond this region rest of both n- and p-type regions remain as usual in a neutral state. This region is the heart of all p – n diode or transistor devices. It has been observed that the depletion region's width and density (ρ) mainly depend on the distribution of immobile ions, with zero charges at the junction. Two different distributions, step-graded and linear-graded doping, are being formulated here (discussed later). If the concentration of acceptor ions (N_A) is different from that of donors (N_D), then space charge is asymmetric about the junction; however, in this case, the charge neutrality condition, as given in equation (1), predicts that the width of space charge is on both sides of the junction.

$$N_D\, x_n = N_A\, x_p \qquad \textbf{(1)}$$

Where x_n and x_p represent the width of the space charge in the n-type and p-type regions, respectively; this particular relation has assumed zero free carriers within the depletion region.

As mentioned earlier, for any p – n diode, the charge distribution of the depletion region plays the most crucial role in the current-voltage characteristics. Herein, this distribution constitutes a layer of an electric dipole, giving rise to electric lines of flux from immobile positively charged donor ions of the n-type region into immobile negatively charged acceptor ions of the p-type region (shown in Fig. **2**). Thus, the built-in – electric field ($\xi_{\text{built-in-potential}}$) plays the most important role in every charge transport characteristic through the p – n diode. However, in this

CHAPTER 3

Metal Semiconductor Contacts Schottky Diodes

Abstract: Metal-Semiconductor-Junction is also called heterojunction since the material on each side of the junction is not identical. The normal pn junction diode concept can also be applied here. There are two probable types of metal-semiconductor junctions: Schottky junction and ohmic junction. When the work-function of metal is greater than the work-function of a semiconductor, then this is called Schottky junction. Ohmic junctions are the junctions in which the work function of the metal is less than the work function of a semiconductor. Their band engineering discussed in detail the essentials of junction physics.

Keywords: Band engineering, Heterojunction, Schottky contact, Ohmic contact.

INTRODUCTION

Semiconductor materials are homogeneous throughout the structure, called a **semiconductor homojunction**. Similar energy bandgaps are the prime factor that is to be noted in homojunction. On the contrary, two different semiconductor materials are there to form a junction; then, it is called **semiconductor heterojunction.** In heterojunction, a combination of narrow bandgap material with wide bandgap material is found. Fig. (**1**) shows three probable combinations. When the forbidden band gap of wide bandgap material completely overlaps with the narrow bandgap materials, it is called straddling. A portion of the wide bandgap and narrow band gap overlap in staggered. In a broken gap, there is a bandgap itself that exists between the energy band gaps of two dissimilar semiconductors.

Metal-Semiconductor Junction

A good example of heterojunction is the Metal-semiconductor junction. This junction can be formed by depositing a metal (Al, Au, Ag, *etc*.) over a semiconductor. Deposition techniques may vary, like e-beam/thermal evaporation, sputtering, CVD, etc. Based on the work function of the metal, the type of junction varies, that is, the ohmic or Schottky junction. As the name suggests, if the contact

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is ohmic, the current-voltage relationship is linear, and also, it is mandatory that the semiconductor is heavily doped because the metal work function is lesser than the semiconductor work function.

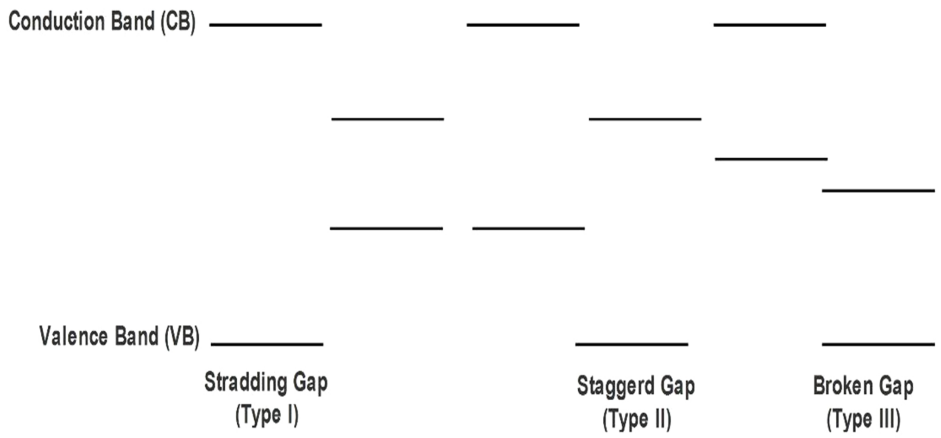

Fig. (1). Different types of heterojunction (**a**) straddling (**b**) staggered (**c**) broken gap.

So, Schottky diodes are formed by depositing metal over a lightly doped semiconductor. Schottky junction switches faster than pn junction as in Schottky junction, majority carriers only dominate, and there is the depletion region on one side of the junction only.

The band chemistry [1-3] of a metal-semiconductor junction can be best understood by the energy band diagram to comprehend the electronic transport throughout the junction. Prior to that, the following factors are to be noted:

Work Function (Φ)

Work function is the most important parameter in understanding band chemistry. It is the gap between the vacuum level and the Fermi energy level of any energy band diagram and is symbolized by φ. It is the least energy required to diffuse one electron from a particular node in a solid to a node just outside its surface. For metal, it is denoted by φ_m or $q\varphi_m$, and for semiconductors, it is denoted by φ_s or $q\varphi_s$, where q indicates the charge of the electron. Work function and ionization energy

are the same in metal. It is not constant for a particular metal as the location of the Fermi level may vary when doping concentration changes. Typical values of φ_m are given in the table below. Surface contaminations are mainly responsible for the varied work function. The photoemission spectroscopy (PES) technique is used to calculate the work function in a semiconductor.

Electron Affinity (χ)

Electron affinity of a semiconductor material can be defined as the energy needed out of an electron from the bottom of the conduction band to the vacuum. The vacuum level indicates the energy level of an electron when it is absolutely free. Electron affinity is denoted by χ or $q\chi$, where q indicates the charge of the electron. The unit is an electron volt (eV). It is a native property of a material and doesn't depend on doping, as the vacuum level, and the lower of the conduction band can't be changed. Table **1** gives the value of the work function of some metals.

Band Diagram

$\Phi_{ms} = \Phi_m - \Phi_s$= metal semiconductor work function difference or just the difference between two Fermi levels and can't be zero as the average energy of an electron present in the metal is not the same as the average energy of an electron present in the semiconductor.

Table 1. Examples of some metals.

Work Functions of Some Metals	
Element	**The Work Function, φ_m(volt)**
Ag, silver	4.26
Al, aluminum	4.28
Au, gold	5.1
Cr, chromium	4.5
Mo, molybdenum	4.6
Ni, nickel	5.15
Pd, palladium	5.12
Pt, platinum	5.65
Ti, titanium	4.33

CHAPTER 4

Junction Field Effect Transistor

Abstract: FET is a resistor whose resistance value is controlled by the potential applied to the control terminal termed as Gate. The conducting region is called a channel which may be either p type or n type based on the substrate used. The channel conductivity mainly depends on the gate region. I-V characteristics are expressed in a detailed manner with necessary equations. JFET parameters are another crucial factor to understand its characteristics. The small signal model of JFET is illustrated in a very lucid manner.

Keywords: Structure, Structure, Working principle, I-V Characteristics**.**

INTRODUCTION

In 1952, William Shockley first proposed Field Effect Transistor (FET). Unlike bipolar transistors, where minority carriers determine the electrical characteristics, the field effect transistor is a majority carrier device. It is a unipolar device, which means the current conduction is due to the majority of carriers only. FET is a voltage-controlled device. Output current is controlled by an electric field, hence the name field effect transistor.

FET Fundamentals

Three terminals of FET are the source, drain and gate. The source is the terminal through which the carriers enter the channel. The drain is the terminal through which carriers leave the channel. Gate modulates the channel conductivity by the application of voltage to its terminal [1-3]. The following are the useful characteristics of FET.

Source:

- The Source terminal in a Field Effect Transistor is the one through which the carriers enter the channel.

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- This is analogous to the emitter terminal in a Bipolar Junction Transistor.
- The Source terminal can be nominated as S.
- The current entering the channel at the Source terminal is indicated as IS.

Gate:

- Gate terminal controls the channel current.
- Smearing an external voltage at the Gate terminal, the current through it can be made precise.
- Gate is heavily doped.
- The channel conductivity is said to be modulated by the Gate terminal.
- This is analogous to the base terminal in a Bipolar Junction Transistor.
- The Gate terminal can be designated as G.
- The current entering the channel at Gate terminal is indicated as I_G.

Drain:

- The Drain terminal in a Field Effect Transistor is the one through which the carriers leave the channel.
- This is analogous to the collector terminal in a Bipolar Junction Transistor.
- The Drain to Source voltage is designated as V_{DS}.
- The Drain terminal can be designated as D.
- The current leaving the channel at Drain terminal is indicated as I_D.

FET has Several Advantages over BJT

(i) It is a high input impedance device of about 100 Megaohms and above.
(ii) FET has no offset voltage when used as a switch, unlike BJT.

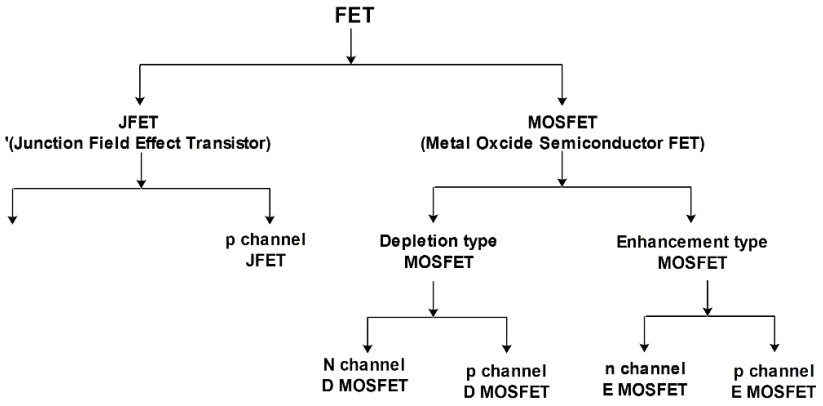
(iii) FET is relatively immune to radiation, but BJT is very sensitive.
(iv) It is a majority carrier device.
(v) FET is less noisy compared to BJT. It is more suitable for input stages of low-level amplifiers.
(vi) FET provides greater thermal stability compared to BJT.
(vii) FET is a unipolar device.

Following are the main disadvantages (demerits) of FETs

(i) FET has a relatively small gain bandwidth product compared to BJT.
(ii) FET suffers from greater susceptibility to damage and hence requires careful handling.

The Field Effect Transistor (FET) can be Broadly Classified into the Following Categories

As Scheme **1** illustratres



Scheme 1. The classification of Field Effect Transistor (FET).

To prefer a FET over BJT, there should be a few advantages to using FETs, rather than BJTs. Let us try to summarize the advantages of FET over BJT. BJT as mentioned in Table **1**.

CHAPTER 5

Metal Oxide Field Effect Transistor (MOSFET)

Abstract: More or less than 17 years since D. Kahng and M. M. Atalla first conveyed the demonstration of a Si-SiO_2 MOS transistor (MOSFET). In our regular lives, the impression of these MOS-based IC's was imparted -just beginning to be felt. This incredible explosion has been caused by many inventions and countless numbers of perhaps small but crucial contributions by many researchers. Historical signs of progress of the metal-oxide-semiconductor field-effect transistor (MOSFET) during the last 60 years are appraised, from the 1928 patent disclosures of the field-effect conductivity modulation concept and the semiconductor triodes structures proposed by Lilienfeld to the 1947 Shockley-originated efforts which controlled to the laboratory demonstration of the modern silicon MOSFET 30 years later in 1960. A review is then made of the mileposts of the past 30 years leading to the latest submicron silicon logic CMOS (Complementary MOS and BICMOS (Combination of Bipolar-junction-Transistor and CMOS) arrays and the three-dimensional and ferroelectric extensions of Dennard's one-transistor dynamic random access memory (DRAM) cell. This chapter discusses the fabrication of MOSFET and its principal operations based on the concept of metal-oxide-semiconductor technology. Further, the discussion is focused on the details mathematical modeling of MOS capacitors, device characteristics, and the process of channel length modulation and its application. The conversation is continuing on the concept of CMOS technology and its combination with the transistor – the BiCMOS technology.

Keywords: BiCMOS, CMOS, MOSFET, Ideal MOS Capacitor, Polysilicon, Threshold Voltage, Long and Short channel MOSFET.

INTRODUCTION

In the present chapter, we discuss the basic operation of one of the most widely used electronic device, particularly in the digital integrated circuit because of its relatively small size, millions of devices can be fabricated in a single integrated circuit. The device has four terminals: source, drain, gate, and bulk body (substrate). Current in the channel can be controlled by applying a voltage to the gate electrode which is isolated from the channel by an insulating material. The resulting device

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is called either Metal-Insulator-Semiconductor (MIS) FET or an Insulated gate field-effect transistor (IGFET). Since most such devices are made using silicon semiconductors, SiO_2 for the insulator, and heavily doped silicon material (polysilicon) for the gate electrode and hence the term metal oxide semiconductor field-effect transistor (MOSFET) is commonly used. This is composed of a MOS diode and two p-n junctions placed immediately adjacent to the MOS diode. The first MOSFET of the silicon substrate using SiO_2 as the gate-insulating material was fabricated in 1960 by Kohang and Atalla. The MOSFET is a fundamental building block of MOS and CMOS digital integrated circuits. Although the MOSFET device is slower than the bipolar transistor but occupies a relatively smaller area on the chip, their fabrication used to involve fewer processing steps [1-3]. The technological advantages together with the relative simplicity of MOSFET operation, have helped to make the MOS transistor the most widely used switching device in LSI and VLSI circuits. However, just like the bipolar circuits, single-polarity MOSFET circuits suffered from a large standby power dissipation and were limited in the level of integration on a chip [3].

MOS Diode

In practical application, the MOS diode is the heart of the MOSFET, which is the most important device for integrated circuits. MOS diode can be used as a storage capacitor in integrated circuits and forms the basic building block for charge-coupled devices (CCD). A perspective view of the MOS diode is shown in Fig. (**1**). The structure consists of three layers: the metal gate electrode, the insulating SiO_2 layer, and the bulk semiconductor (p-type for n-type MOSFET), called substrate or body. This structure is similar to a parallel plate capacitor, where two plates (one of metal and the other one is a semiconductor) are separated by SiO_2 insulating material of thickness t_{ox}. Such MOS structure is thereby also called the MOS capacitor; the carrier concentration and the local distribution within the semiconductor substrate can be manipulated by the external voltage applied to the gate and the substrate terminals.

FABRICATION OF N-MOS

The fabrication of n-channel metal oxide semiconductors (N-MOS) is less complex and requires a minimum number of lithographic processes. For the fabrication of the n-MOS transistor, the following steps are to be followed:

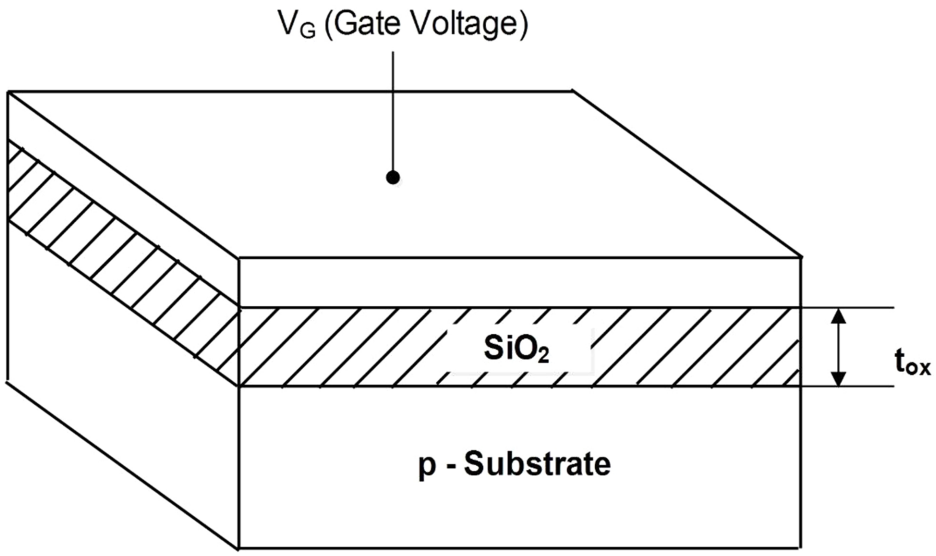

Fig. (1): Perspective view of MOS diode.

Selection of Substrate

The starting material that is required is a silicon substrate, as this fabrication is for an n-MOS, for that reason, a lightly doped p-type silicon substrate will be chosen [4-6]. A thick layer of SiO_2 (~ 1 μm) is grown over the entire top surface of this substrate material by the thermal oxidation method are shown in Fig. (**2**). This SiO_2 layer also acts as a shield to protect the Si substrate from any type of damage.

Deposition of Photoresist

After that, the oxide surface is coated with a uniform layer of positive photoresist material (Fig. **3**). A photoresist is basically a light-sensitive and acid-resisting inorganic polymer. When the photoresist is exposed to light, then its property will be changed. Depending upon this change in property, it is categorized as a positive or negative photoresist. Basically, a positive photoresist is soluble in light during exposure to UV rays, whereas a negative photoresist is initially insoluble in nature but insoluble during exposure to UV rays.

CHAPTER 6

Semiconductor Devices

Abstract: Semiconductor materials are beneficial in their performance and can be easily deployed by the addition of impurities known as doping. The resistivity of the semiconductor can be changed by incorporating the electric or magnetic field, light or heat, or mechanical distortion. Therefore, semiconductors can make excellent devices. Current conduction in a semiconductor happens due to free electrons and holes, jointly known as charge carriers. Doping of silicon significantly increases the number of electrons or holes within the semiconductor, making it "p-type" or "n-type." This doping characteristic is a blessing to make a possible number of devices like LED, Tunnel diode, Solar cells, and many more, which have been discussed in this section.

Keywords: DIAC, LED, PIN Diode, Tunnel diode, Thyristor, TRIAC, Solar Cell.

INTRODUCTION

Semiconductor devices are at the core of the existing industrial revolution and are gradually increasing prominent entities in our daily lives. This chapter develops the basic concepts necessary to comprehend the fundamentals of semiconductor devices [1,2,3]. Learners will apply these notions to gain insight into the operation of various semiconductor devices, such as PN junction diode, PIN diode, LED, and solar cells.

PIN Diode

Although diodes with a simple PN junction are the most common, various types of diodes can be employed in various applications. The PIN diode is one type that is utilized in several circuits. This type of diode is used in a variety of applications. PIN diodes are excellent for RF switching, and the PIN structure is also helpful in photodiodes.

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A photo-detector (photodetector or photo-diode) is another application for the PIN diode, as its structure is well adapted to absorbing light.

Structure and Working of PIN Diode

The term PIN diode has been derived from the fact that it is composed of three main layers, as shown in Fig. (**1**). The PIN diode consists of semiconductor diodes having three layers:

- P-type layer
- Intrinsic layer
- N-type layer

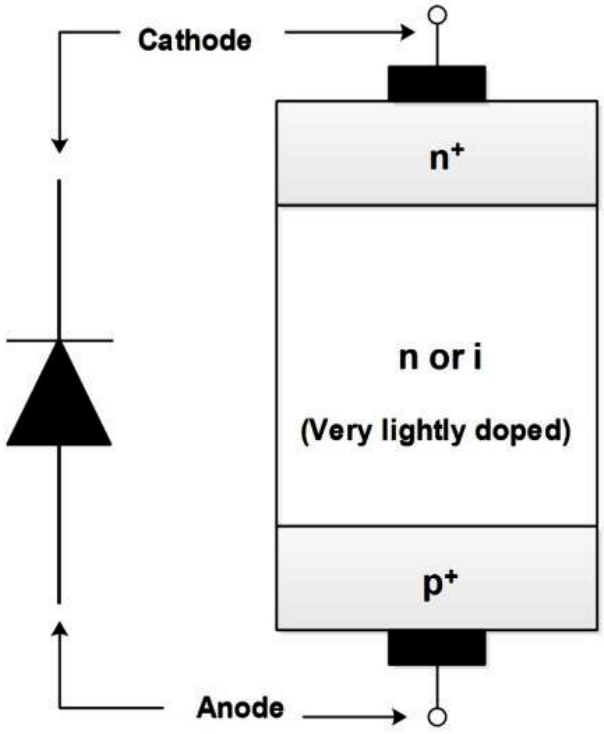

Fig. (1). PIN diode cross-sectional view

The working principle of the PIN diode is closely related to an ordinary PN junction diode. The main difference is that the depletion region, which usually exists between the P & N regions in a reverse-biased or unbiased diode, is larger than the normal PN junction diode. In any PN junction diode, the P region contains holes as

it has been doped to ensure that it has a majority of holes. Likewise, the N-region has been doped to hold excess electrons.

Characteristics PIN Diode

The intrinsic layer between the P-type and N-type regions of the PIN diode allows it to have qualities like a high reverse breakdown voltage and low capacitance, as well as other properties like carrier storage when forward biased, which make it suitable for microwave applications. According to the findings, the depletion layer becomes totally depleted at low levels of reverse bias. As the intrinsic layer has a little net charge, the capacitance of a PIN diode is independent of the bias level until it is entirely depleted. However, because the capacitance is often lower than other types of diodes, any RF signal leakage across the diode is minimized.

Both current carriers are injected into the intrinsic layer when the PIN diode is forward-biased, where they mix. The current can pass over the layer because of this procedure. When utilized with high-frequency signals, the PIN diode looks like a resistor rather than a nonlinear device and thus causes no rectification or distortion. The DC bias applied determines its resistance. As a result, the device can be used as an effective RF switch or variable resistor with significantly less distortion than standard PN junction diodes.

PIN Diode Applications and Benefits

The PIN diode is used in several areas based on its structure. There are some properties of PIN diode which are of particular use.

Microwave Switches

Due to their low capacitance, the PIN diode can be used as a microwave switch. When the device's n-type terminal is positive in relation to the p-type terminal, charge carriers flow from the intrinsic layer to the n-type layer. As a result, the intrinsic layer's effective charge carrier is insignificant. There is no energy dissipation in the intrinsic layer in this situation. The resistance of the diode grows to a few kilo-ohms in this state, known as the OFF state. Current flows through the diode when the device is forward-biased, and power is generated from the signal source. This is known as the ON state.

CHAPTER 7

Silicon

Abstract: This chapter introduces silicon as an electronic material for microelectronic device fabrication. It discusses, in-depth, the various aspects of crystalline silicon, wafer manufacturing and their identification techniques. Finally, the various steps involved in a microfabrication process are also discussed. From this chapter, the readers are expected to learn how to process a silicon wafer successfully and proceed with customized device fabrication.

Keywords: Silicon, Microfabrication, Crystal, Miller indices, Ingot, Wafers.

INTRODUCTION

The basic yet most significant electronic device for integrated circuits is the metal oxide semiconductor field effect transistor (commonly abbreviated as MOSFET) since its discovery in 1960 [1]. One such primitive device had a gate length of 20 μm and an oxide thickness of 100 μm. Since then, silicon technology has taken a toll and developed at an exponential rate. As of 2020, NVidia's GA100 Graphics Processing Unit (GPU), consisting of 54 billion MOSFETs, demonstrated the highest transistor count in a single chip which was manufactured using Taiwan Semiconductors Manufacturing Company's (TSMC) 7 nm process. Silicon, being the second most abundantly found element as well as an excellent semiconductor, has completely dominated the electronic manufacturing industry for more than three decades. As a device engineer, it is very important to know the basics of a semiconductor device fabrication process, starting from silicon manufacturing and processing to etching and lift-offs. With time, semiconductor fabrication has improved significantly with increasing consumer demands, miniaturization and other industrial factors like market competition, urge to integrate more features, user-friendliness, etc. Here, we will introduce you to silicon, its crystallography, its optical and electronic properties, and its manufacturing and processing strategies [1]. This chapter would set the foothold for any complex device fabrication strategy that may follow.

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Crystal Systems

Solids may exist in several atomic arrangements. Based on the nature of these arrangements, they are broadly subdivided as (i) crystalline – where there exists a periodic arrangement of atoms throughout the entire material, (ii) semi-crystalline– where the periodic arrangement exists but not throughout the material and (iii) amorphous where there is no periodic arrangement of atoms. Most semiconductors are crystalline in nature, following a specific crystal geometry. The following section will introduce to the readers the basic concept of crystallography, its origin, formation and existence [2].

Since there are many different possible crystal structures, it is sometimes convenient to group them according to unit cell configurations. In this regard, the unit cell of a crystal is defined as the smallest repeat entity consisting of a periodic arrangement of atoms which describes the crystal structure on its repetition in the three crystallography axes. Fig. (**1**) below demonstrates a basic crystal lattice formed of a unit cell.

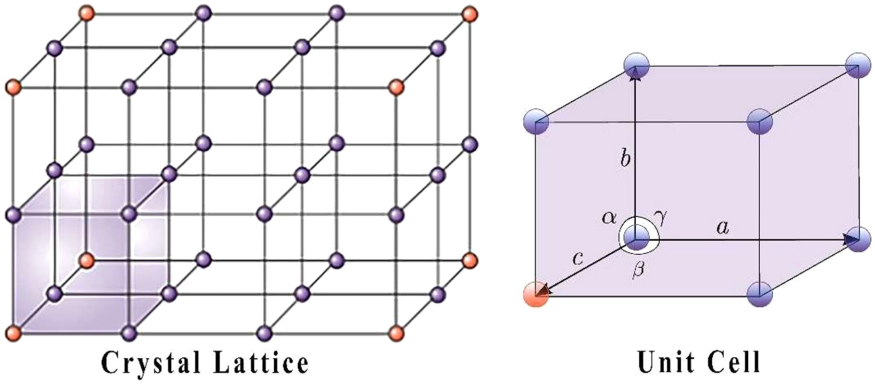

Fig. (1). Illustration showing a crystal lattice formed by a unit cell. The unit cell has sides a, b and c and angles α, β and γ.

Unit cells for most crystal structures are parallelepipeds or prisms having three sets of parallel faces: one is drawn within the aggregate of spheres, which in this case happens to be a cube. A unit cell is chosen to represent the symmetry of the crystal structure, wherein all the atom positions in the crystal may be generated by translations of unit cell integral distances along each side of its edges. Thus, the unit cell is the basic structural building block of a crystal and defines it by virtue of

its geometry and atomic positions within it. It is convenient enough to dedicate the centre of the hard-sphere atoms to each corner of the parallelepipeds. Furthermore, multiple single-unit cells may be chosen for a definite crystal structure; however, the unit cell with the highest geometrical symmetry level is generally used.

Crystal Systems and Miller Indices

In a crystal unit cell, when viewed in three dimensions, several planes can be isolated. The atomic spacing in each of these planes is different. Therefore, the crystal properties along different planes will also vary, thereby affecting the electrical and other device characteristics. Thus, it is important to estimate the crystal orientation. A convenient method of defining such planes is by using miller indices. The following steps demonstrate the determination of a crystal plane by estimating the Miller indices. These are as follows:

1. Find the intercept of the plane in three Cartesian coordinates in terms of the lattice constants.

2. Take the reciprocal of these numbers and reduce them to the smallest three integers keeping the ratio same.

3. Represent the numbers as (h k l) which represents the Miller indices for a single plane.

Types of Crystal Structures

Complex crystal structures are formed of relatively simple crystal units which are found in most common metals and semiconductors. Three such units which are commonly encountered are: face-centred cubic, body-centred cubic and hexagonal close-packed.

Face-centred Cubic Crystal Structure

The crystal structure found for many metals has a unit cell of crystal geometry, with atoms located at each of the corners and centres of all the cube faces. This is called the face-centred cubic (FCC) structure. Some of the familiar metals having this crystal structure are copper, aluminium, silver and gold. Fig. (**2**) shows a hard sphere model for FCC unit cell where the atoms centres are represented by red spheres and those in the corners by yellow spheres. These spheres touch one another

CHAPTER 8

Oxidation

Abstract: This chapter introduces the readers to the oxidation process focusing on silicon. It establishes the importance of oxidation in a silicon process and discusses the thermal oxidation process and its growth mechanism in depth. Towards the end, a detailed discussion on the oxide film characterization and its properties is provided. After reading this chapter, the readers are expected to have a sound knowledge of the oxidation process as a whole and its significance in the silicon processing industry.

Keywords: Oxidation, Silicon dioxide, Deal-Grove Model, Kinetics, Thin film oxides, Oxide-induced defects.

INTRODUCTION

Discrete devices and integrated circuit fabrication involve the use of different types of thin films. These may be classified as thermal oxides, dielectric layers, polycrystalline silicon and metal films. Fig. (**1**) shows a schematic view of a conventional silicon n – channel metal–oxide–semiconductor field–effect transistor (MOSFET) using all four types of films. The most important film from the thermal oxide group is the gate–oxide layer, under which the conducting channel is formed between the source and the drain regions. Both gate and field oxides are generally grown by the thermal oxidation process, providing the highest–quality oxide with the lowest interface trap densities [1].

Dielectric layers such as silicon dioxide (SiO_2) and silicon nitride (Si_3N_4) are used as insulators between conducting layers mostly as diffusion and ion implantation masks, for capping doped films to prevent dopant loss and for passivation to protect devices from impurities, moisture and scratches. Polycrystalline silicon, usually referred to as polysilicon, is used as a gate electrode material in MOS devices. Polysilicon is a conductive material for multilevel metallization and a contact material for devices with shallow junctions. Metal films, *e.g.*, copper and silicides,

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are used to form low–resistance interconnects, ohmic contacts, and rectifying metal-semiconductor barriers.

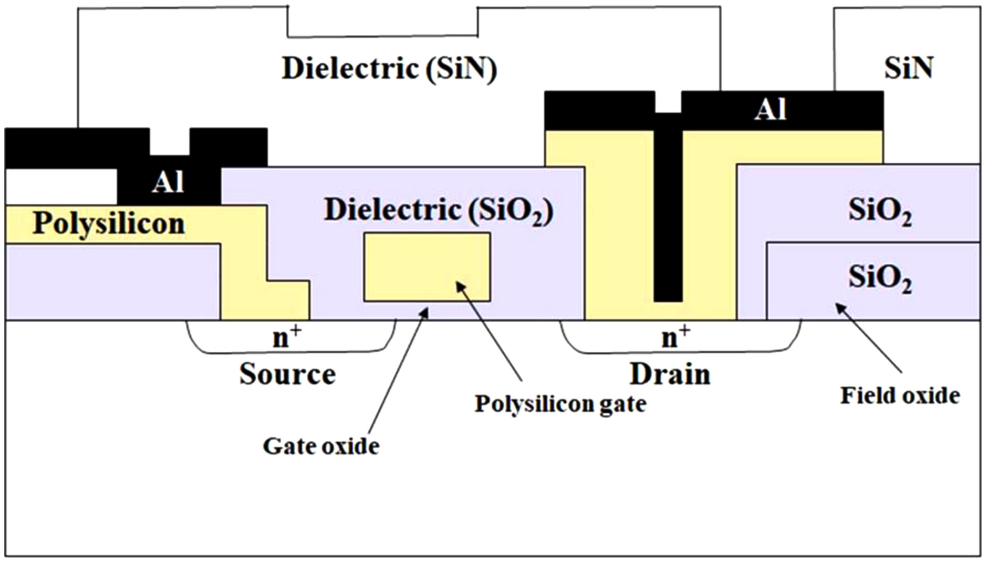

Fig. (1). Schematic cross-section of a metal–oxide–semiconductor field–effect transistor.

Thermal Oxidation

Oxidation in semiconductors can be performed in a plethora of methods. These include thermal oxidation, electrochemical anodization and plasma reaction. Among these, thermal oxidation is by far the most important for silicon devices. It is the key process in modern silicon integrated circuit–technology. For gallium arsenide (GaAs), however, oxidation generally results in non–stoichiometric films. The oxides provide poor electrical insulation and semiconductor surface protection, and hence, these oxides are rarely used in the GaAs technology. In the following section, we will focus on the thermal oxidation of silicon wafers.

Fig. (**2**) demonstrates a basic thermal oxidation furnace. The reactor consists of a resistance–heated furnace, a cylinder-fused–quartz tube containing the silicon wafers held vertically in a slotted quartz boat, and a source of either pure dry oxygen or water vapour (Fig. **3**).

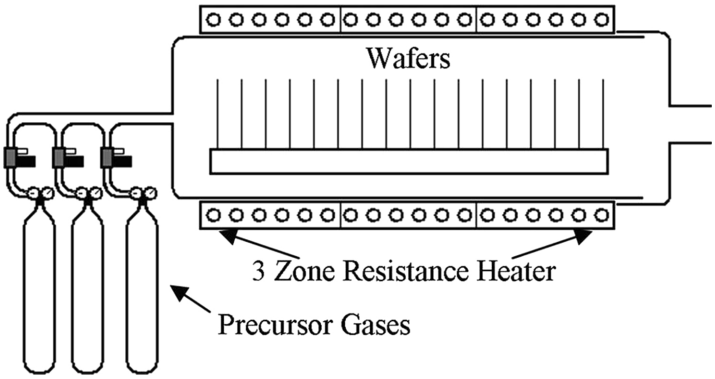

Fig. (2). Schematic of a resistive heating thermal oxidation furnace

Fig. (3). Insertion of pure silicon wafers into a thermal oxidation chamber stacked in a slotted quartz wafer holder

The loading end of the furnace tube protrudes into a vertical flow hood where a filtered flow of air is maintained. The hood reduces dust and particulate matter in the air surrounding the wafers and minimizes contamination during wafer loading. The oxidation temperature is generally kept at 900 – 1200oC, and the typical gas flow is around 1 litre/min. The operation of the furnace is often fully automated with a microcontroller-assisted control unit. It controls the sequence of the gases, gas flow rate, automatic insertion and removal of Si wafers and temperature ramping (i.e., increase of temperature furnace linearly) from a low temperature to the oxidation temperature so that the wafers will not warp due to sudden temperature changes, to maintain the oxidation temperature to within ±1oC, and to ramp down the temperature after the oxidation is completed.

CHAPTER 9

Diffusion

Abstract: This chapter introduces the readers to the diffusion process of doping intrinsic silicon. It discusses Fick's Law of diffusion in-depth and the different types of diffusion that may be observed. Towards the latter part of the chapter, the diffusion process in semiconductors has been discussed in detail, explaining the diffusion-assisted doping process commonly employed for semiconductors, especially silicon.

Keywords: Fick's Law, Interstitial, Vacancy, Diffusion flux, Steady-state diffusion, Drive-in diffusion.

INTRODUCTION

Many critical reactions and processes in handling materials rely on mass transfer from a liquid, a gas, or another solid phase to a specified solid (usually on a microscopic level). The diffusion process accomplishes this. Diffusion is a material transport phenomenon facilitated by atomic mobility. The atomistic mechanisms that cause diffusion, the rate equation, diffusion mathematics, measurement methodologies, and diffusion in silicon dioxide and polysilicon are all covered in this chapter.

The diffusion phenomena are best represented using a diffusion couple, which is made by attaching two metal bars to make close contact between the two faces, as shown in Fig. (**1a-f**), which includes schematic representations of atomic locations and composition across the interface. This pair is heated to a high temperature (but below the melting temperatures of both metals) for a long time before being cooled to room temperature. As a result of such high-temperature exposure, chemical examination indicates a situation similar to that shown in Fig. (**1b**), pure copper and nickel at the two extremities of the pair, separated by an alloyed zone. The concentrations of both metals, on the other hand, fluctuate depending on the position. Copper atoms migrate into nickel and vice versa in this diagram. Interdiffusion, also known as impurity diffusion, is a type of diffusion. Changes in

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concentration over time, as in the case of the Cu–Ni diffusion couple, can be used to detect interdiffusion from a macroscopic perspective. Atoms are transported from high- to low-concentration regions in a net drift. Pure metals may also experience diffusion. Self-diffusion occurs when all diffusing particles exchanging locations are of the same type. On the other hand, self-diffusion isn't usually observed by noticing compositional changes [1].

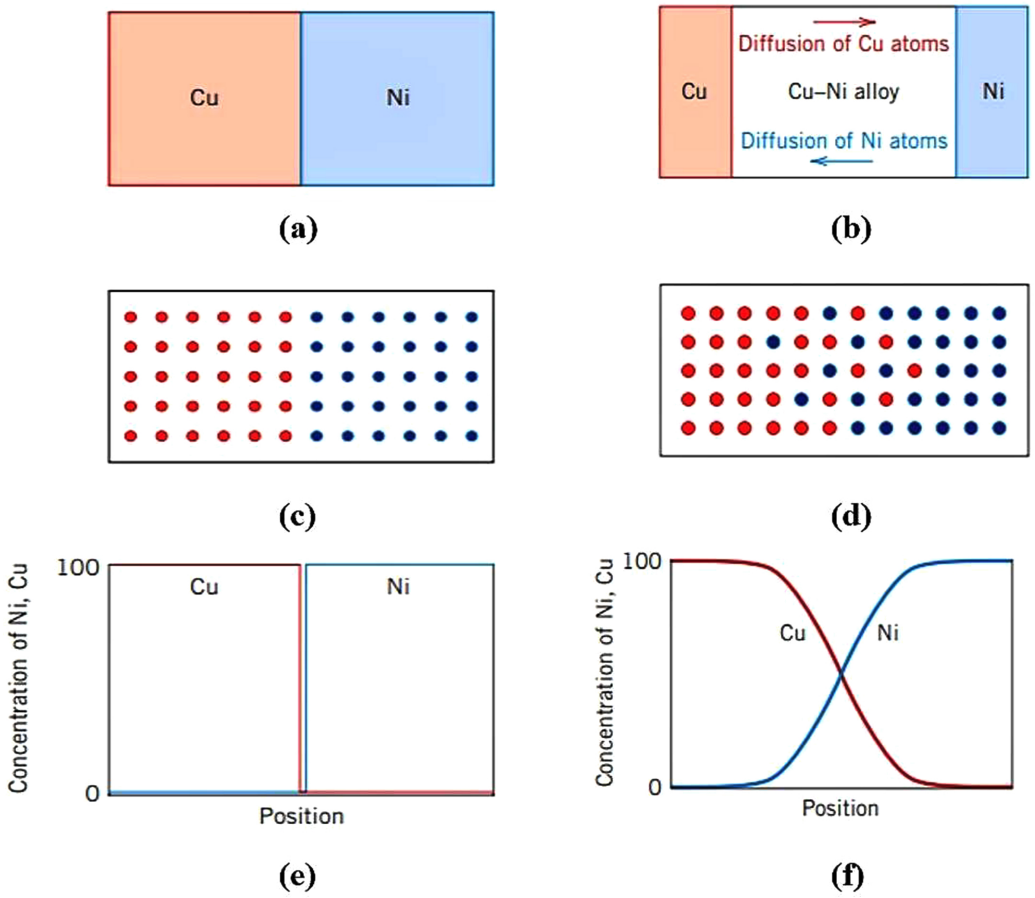

Fig. (1). (a) – (b) A Cu–Ni diffusion couple before and after high heat treatment (**c**) – (**d**) Schematic representation of copper atoms (in red) and nickel atoms (in blue) within the diffusion couple before and after diffusion (**e**) – (**f**) Concentration of copper and nickel atoms as a function of position throughout the length of the diffusion couple before and after diffusion

Mechanisms of Diffusion

From the atomic perspective, diffusion is the systematic migration of atoms between two or more lattice sites. It is well known from the kinetic theory of matter in solids that the constituent atoms of the solid are in constant motion, rapidly changing their positions. For an atom to make such a move, two conditions must be achieved: (1) the existence of an empty adjacent site, and (2) the vibrating atom must have sufficient energy to break bonds with its neighboring atoms to create some lattice distortions during the displacement. This energy is vibrational. At a particular temperature, only a tiny fraction of the total number of atoms is capable of such diffusive motion by the magnitudes of their vibrational energies, which increase with rising temperature. Different models have been proposed for this atomic motion; among these, the following two models dominate for metallic diffusion.

Interstitial Diffusion

Atoms migrate from one interstitial place to a nearby one unoccupied in this sort of diffusion. The interdiffusion of impurity atoms such as hydrogen, carbon, oxygen, and nitrogen, which have tiny particles that easily fit into the interstitial locations, is commonly observed by this method. Interstitials are rarely formed by substitutional or host impurities, and they are seldom dispersed through this process. Interstitial diffusion is the proper name for this phenomenon because it involves interstitials. Interstitial diffusion is substantially faster than vacancy diffusion in most metal alloys because the interstitial atoms are smaller and more mobile. Furthermore, there are many more unfilled interstitial places than vacancies, implying that interstitial atomic migration is considerably more likely. This is depicted in Fig. (**2**) below.

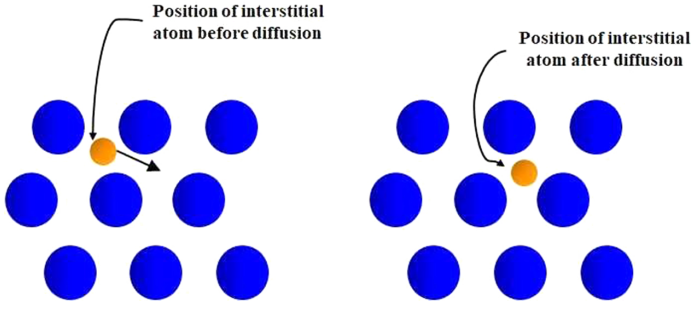

Fig. (2). Schematic representation of interstitial diffusion.

CHAPTER 10

Ion Implantation

Abstract: This chapter discusses the ion implantation process of silicon processing technology in depth. The chapter gives an in-depth insight into various aspects of the ion implantation process and ion-implanted silicon systems commonly encountered in a silicon process. After reading this chapter, the readers will have a sound understanding of the ion implantation process and its various aspects.

Keywords: Buried layer, Channeling, Ion implantation, Ion stopping, Range theory, Recoils.

INTRODUCTION

Ion implantation may be termed a low-temperature process to introduce dopants (impurities) into a semiconductor lattice, offering more flexibility than diffusion. It is often used to fine-tune the device performance; for example, in MOS transistors, ion implantation can be accurately employed to tune the device threshold voltage. In ion implantation, dopant atoms are volatilized, ionized, separated, or accelerated by the charge-to-mass ratios and directed towards a silicon substrate (the target). The atoms entering the crystal lattice eventually stop colliding with the host atoms by losing energy at a depth within the crystal. The substrate materials, dopant, and acceleration energy determine the average penetration depth. Ion implantation energies can range from a few hundred to several million electron volts, resulting in an ion dispersion profile with typical depths of less than ten nanometres to ten meters. Doses for threshold adjustment range from 10^{11} atoms/cm^2 to 10^{18} atoms/cm^2 for buried dielectric production [1].

Range Theory Ion Stopping

A dopant ion collides with the host atoms multiple times before stopping at a certain depth while impinging on the target. Ion scattering is mainly based on elastic collisions between nuclei pairs. The initial ion energy is often in the tens of KeV

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range, which is significantly greater than lattice binding energies, and the comparatively weak lattice forces are neglected. Inelastic collisions with electrons in target atoms, on the other hand, may produce a second scattering component. As a result, the total stopping power S is defined by the energy loss (E) per unit path length (x) of the ion and is equal to the sum of the nuclear and electronic interactions as follows:

$$S = \left(\frac{dE}{dx}\right)_{\text{nuclear}} + \left(\frac{dE}{dx}\right)_{\text{electronic}} \quad \textbf{(1)}$$

Fig. 1 shows the relative distribution to S and the position of each term over a wide energy range. The Figure demonstrates that ion implantation energies, ranging from 10 to 200 KeV, fall on the far left, dominated by nuclear stopping [2].

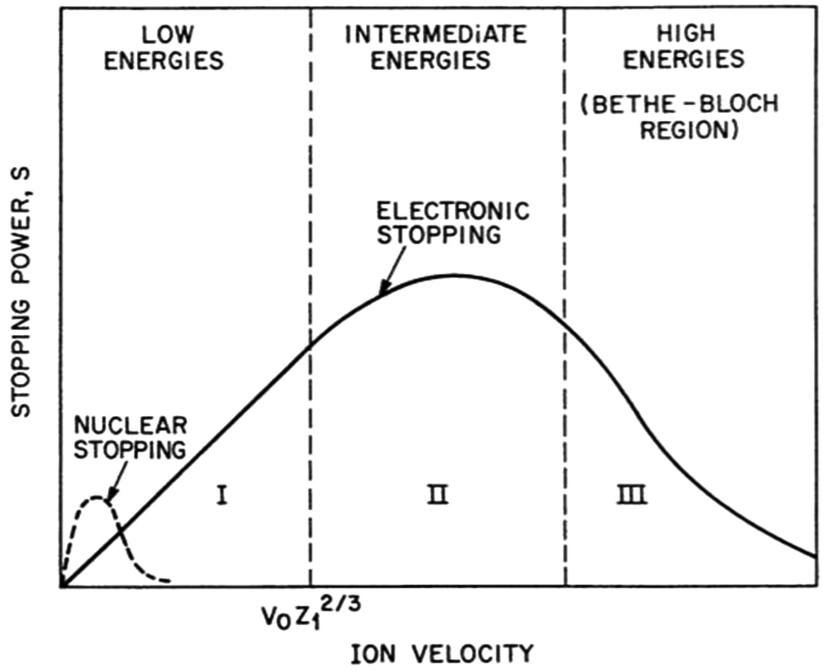

Fig. (1). The ion stopping power's nuclear and electronic components function as ion velocity. The quantity v_o is the Bohr velocity, oη q/4πε0h, and Z_1 is the ion atomic number.

As explained by classical kinematics, nuclear halting is the most common result of a collision between two atoms. Assuming the atoms are bare nuclei, the columbic potential between them at a distance r would be:

$$V_c(r) = \frac{q^2 z_1 z_2}{4\pi s_0 r} \quad \textbf{(2)}$$

ε_0 is the permittivity, and q is the electronic charge, where z_1 and z_2 are the atomic numbers of the implanted and target atoms, respectively. As electrons screen the nuclear charge, a screening function, $f_S(r)$, must be included:

$$(r) = V_c(r) f_s(r) \quad \textbf{(3)}$$

The equations of motion of atoms can be integrated to derive the scattering angle of any incident ion trajectory given the contact potential. Using the center-of-mass frame, the following result can be obtained:

$$T = \frac{4M_1M_2}{(M_1 + M_2)^2} E \sin^2\left\{\frac{\theta}{2}\right\} \quad \textbf{(4)}$$

T is the energy lost by the incoming ion, E is the ion's energy, is the scattering angle, and M_1 and M_2 are the ion's and target atom's atomic mass numbers, respectively. Integrating the loss of energy multiplied by the likelihood of occurrence of one specific collision yields the rate of energy loss due to nuclear collisions per unit travel length. If 'T_{max}' is the greatest energy transfer in a single collision and 'N' is the number of target atoms per unit volume, then

$$S_n = \left(\frac{dE}{dx}\right)_{nuclear} = N \int_0^{T_{max}} T d\sigma \quad \textbf{(5)}$$

The differential cross-section is denoted by d. Due to the elasticity of nuclear stopping, the energy lost by the bombarding ion is transmitted to the target atom and then recoiled away, causing a defect in the lattice site.

The interaction between the electrons in the target and the incoming ion causes electronic halting. Though the theoretical model is complicated, the stopping is akin to a viscous drag force and proportionate to the ion velocity in the low energy zone. Because electronic stopping is inelastic, the energy lost by incident ions is dissipated into thermal vibrations of the target through the electron cloud.

CHAPTER 11

MEMS in Improved Efficiency

Abstract: Micro-Electro-Mechanical Systems or MEMS, **are** an achievement of this era and revolutionized the semiconductor industry. It is the amalgamation of microelectronics with micromachining technology. Though the term mechanical is one of the keywords of MEMS but not necessarily, micromachined devices should not contain mechanical parts always. Machine means cutting tools. In MEMS technology, the micron-level substrates are cut down to fabricate the device. The primary purpose of MEMS technology is miniaturization with low power consumption. The term MEMS can be described in many ways. In a single sense, MEMS is a platform on top of which some common microscopic mechanical parts, *e.g.,* channels, holes, cantilevers, membranes, cavities, and other structures, can be fabricated. Though micromachining is associated with MEMS, still the structures are not machined. Instead, they are created using micro-fabrication technology suitable for batch processing for integrated circuits.

Keywords: Bulk micromachining, CMOS compatibility, MEMS materials, Surface micromachining.

INTRODUCTION

The most promising aspect of MEMS fabrication is batch processing. In precision engineering, the device is fabricated one by one, not in a group which makes it more expensive. But the batch processing is highly economical; therefore, MEMS adds to the economy in the microelectronics industry.

When choosing the MEMS material, their mechanical properties are much more concerned rather than electrical ones. Mechanical properties encountered in MEMS are - high stiffness, high fracture strength, fracture toughness, and high-temperature stability or chemical inertness, depending on the application.

The basic building block of a MEMS device is the substrate which is nothing but an object with a macroscopic/microscopic surface finish. In semiconductor electronics, the substrate is nothing but a piece of single-crystal silicon with a

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microscopic surface finish commonly known as a wafer. A substrate with a macroscopic surface finish can be of other materials also, *e.g.*, quartz, alumina, GaAs, *etc.* These substrates should have a material quality as high as possible, and at the same time, they should be as cheap in production as possible.

Among them, the main advantage of using semiconductors (Si, Ge, GaAs) as a substrate material is that– they can be used as semiconductors and conductors depending on the industry's requirement. This type of flexibility has been achieved by doping, in which foreign materials are added to the semiconductor to convert them from semiconductors to the electrical conductor. The physics behind it is already elaborated on in different books, so not included in this chapter.

From the technical point of view, the use of semiconductors as a substrate material is that Integration of MEMS and CMOS structures into a truly monolithic device has proven to be highly challenging; all the processes, such as etching, diffusion, deposition, *etc.*, have already been established. However, much evolution continues to be made.

MEMS Materials

Single-crystal silicon (p type/n type) is the principal material in the semiconductor industry. Other used silicon compounds acting as substrate materials primarily are SiO_2, SiC, Si_3N_4, and polysilicon. The polymers can also be used as substrate materials in MEMS and Microsystems technology.

Silicon is an ideal substrate material for MEMS because it can be micromachined by a low-cost wet etching technique. It is abundant material on earth and found in compound form.
Single crystal silicon is prepared in the form of an ingot by some sophisticated technique with the requirement of a high-end laboratory. Silicon is a popular semiconductor material and has already replaced other substrate materials due to following reasons:

1) It is lighter than Al and harder than steel. It has about the same Young’s modulus as steel (~ 2x105 MPa) but is as light as aluminum with a density of about 2.3 g/cm^3.

2) Mechanically it is much more stable.

3) It is an ideal structural material in the microelectronics industry. Miniaturised Mechanical devices can be made with high precision on silicon.

4) It has a melting point of 1400°C, about double that of aluminum. Due to its high melting point, silicon is dimensionally stable even at high temperatures.

5) The thermal expansion coefficient of aluminum is around eight times that of steel and more than ten times that of steel.

6) Silicon does not appear to have mechanical hysteresis. As a result, it's an excellent material for sensors and actuators. The flexibility of silicon is much higher than other substrate materials.

7) The processing steps of silicon are well established and need no further liability.

Other crystalline semiconductors, including germanium (Ge) and gallium arsenide (GaAs), are also used as substrate materials due to their similar features. Still, silicon is much more popular for its distinguished property. Silicon can readily be oxidized to form a chemically inert insulating layer of SiO_2 in a humid oxygen environment.

Silicon is the most used material in integrated circuits. It is also a popular CMOS-compatible material.

It's a good material for making MEMS since it has a lot of beneficial mechanical and chemical properties: Single crystalline silicon is a Hookean material that is nearly flawless. This means there is no hysteresis and, thus, almost little energy is lost when silicon is bent. This feature makes silicon the best material for applications requiring many tiny movements and excellent dependability, as silicon is resistant to fatigue and has service lifetimes in the billions to trillions of cycles. Though silicon is the most popular MEMS substrate, ongoing research and development may uncover non-semiconductor substrate materials, such as metals, glasses, quartz, crystalline insulators, ceramics, and polymers. The ability of today's MEMS substrates to incorporate circuits directly onto the substrate is currently a critical concern.

CHAPTER 12

Lithography

Abstract: A few lithography techniques have been developed in the past few decades with improvements in lens systems and advanced radiation sources for exposure, such as photons, X-rays, electrons, ions, and neutral atoms. With each type of exposure source, the instrumental details significantly change. However, the fundamental principle behind the lithographic approaches remains the same. Photolithography is the most intensive technique in microelectronic fabrication, especially for the bulk production of integrated circuits (ICs). Below the different types of lithography techniques are described in detail.

Keywords: Maskless lithography, Optical lithography, Processes, Soft lithography process.

INTRODUCTION

Photolithography is a photographic method that uses an ultraviolet ray of light to transfer a reproduction of a master design onto a substrate of a different material (typically a silicon wafer).

Surface preparation is critical before applying a photoresist to maximize resist-adherence. As a result, adhesion enhancers are utilized after cleaning to aid resist coating. The following factors have an impact on resist adhesion:

• Moisture content on the surface

• Resist wetting properties

• Primer type

• Delay in exposure and prebake

• Resist chemistry

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• Surface smoothness

• Stress from the coating process

The wafer surface should ideally be free of any water molecules or moisture. Before priming and coating, keeping the wafers in a heating oven is critical. It ought to be.

The main components of a lithographic process are:

• Oxidized silicon wafer
• Photo-resist: light-sensitive carbon polymer
• Photolithographic masks act as a master pattern
• Alignment setup
• Ultraviolet exposure
• Development using developer solution to form the desired pattern of photoresist
• Etching
• Stripping

Optical Lithography

In the lithographic process, the substrate (usually a silicon wafer) is first coated with some oxide layer. A photoresist is a thin layer of an organic polymer sensitive to UV radiation placed on top of the oxide layer. A photomask, made of transparent plastic with a chromium pattern (opaque), is placed on top of the photoresist-coated surface. There are two sorts of masks: black film masks and brilliant film masks. UV radiation is used to expose the wafer. The transparent portion of the mask allows light/radiation to pass through, and the other opaque part blocks it.

Thus, the pattern is transferred to the resist, which is subsequently developed using an organic developer. In exposed portions of the photoresist, UV radiation changes the polymeric bond.

There are two forms of photoresist: positive and negative. UV radiation strengthens positive photoresists while weakening negative photoresists. The developer eliminates the exposed or unexposed portions of the photoresist during development, leaving a pattern on the oxide-covered wafer surface. The photoresist patterns result in either a positive or negative image of the photomask's original pattern. To eliminate the additional metal outside of the exposed portions of the

photoresist, a reagent (typically hydrochloric acid) is utilized. After that, the excess patterned photoresist is removed, usually using acetone.

The inorganic photoresist is presently capturing the market due to nanoparticle (254nm and 193nm) patterning [1, 2].

In the conventional 193nm, the photoresist nanoparticle core is attached with functional groups. Many resist materials degrade in plasma or ion-beam environments.

Diffraction is the most significant restriction in optical lithography. Diffraction does not affect electron beams, so electron beam lithography is not limited by diffraction. In the case of optical lithography, it can also be reduced by using excimer lasers, which produce nanosecond pulses and microscopic patterns—introducing resolution improvement techniques and changing the photoresist chemical.

Properties of Resist

Sensitivity

As photoresists are organic polymers, they are extremely susceptible to radiation, and their chemical characteristics are substantially altered. Even under typical operation light, it is sensitive. That is why it is maintained in a dark room at all times. The increased sensitivity minimizes the exposure time, which significantly impacts the fabrication cost, and resists (either positive or negative) optical lithography response to wavelengths between 330 and 430 nm.

Deep sub-micron lithography has recently attracted much attention since it uses the deep UV area (150 – 300 nm) to provide greater resolution, aiding device shrinking. However, there are significant limitations regarding wavelength selection, as the operation at these shorter wavelengths necessitates a higher frequency.

The photoresist affects the e-beam and X-ray lithography's functionalization (5-50 Å). For the e-beam technique, the resist should be sensitive to electron irradiation in the 10 – 30 KV range for reticle mask generation.

SUBJECT INDEX

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The topics are quite important in the context of recent developments in solid state microelectronics devices and recent teaching curricula. The writers have experience in the area and would be able to do appropriate justice to the topic. I am sure that the book will evoke widespread interest as the field has matured enough to write a fresh book, and is still offering newer possibilities. Readers will be immensely benefited by knowing the fundamentals as well as current and future developments.

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